Automatization of Digital Predistortion and Crest Factor Reduction

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Abstract – Power amplifier (PA) linearization, achieved by utilization of digital predistortion (DPD) technique, improves PA energy efficiency and reduces running cost of telecommunication equipment. In modern modulation schemes, the reduction of the peak to average power ratio of transmitted waveforms is necessary operation which ensures PA linearity. To achieve this, the Peak Windowing and DPD are implemented in Software Defined Radio (SDR) base station. The results are presented for Long-Term Evolution (LTE) waveforms and 10W modulated output PAs.

Keywords - Crest factor reduction, Peak to Average Power Ratio, Peak Windowing method.

I. Introduction

Digital predistortion (DPD), based on complex valued memory polynomials (MP), is established as an efficient method for radio frequency (RF) power amplifier (PA) linearization [1, 2]. However, modern modulation schemes facilitate high peak-to-average power ratio, which results in intercarrier interference, high out-of-band emission and bit error rate performance degradation [1]. Therefore, RF PA power has to be backed-off reducing the PA energy efficiency. To ensure that signals at PA input stay within linear region of the PA transfer function, the solution is in dealing with signals which have reduced PAPR. In this case it is possible to increase signal average power without the risk of PA operation in non-linear region [2]. This solution significantly cuts the running cost of wireless infrastructure.

Crest Factor Reduction (CFR) techniques are used for PAPR reduction [3, 4]. Our method for CFR is based on Peak Windowing (PW) [5]. The combination of DPD and PW PAPR reduction methods is implemented on Software Defined Radio (SDR) board and the results are given in the paper.

II. Methods for PA Linearization

A. Crest Factor Measurement

Crest Factor (CF) a signal *x(n)* is defined as the ratio between the amplitudes related to the largest $x(n)_{\max}$ and the mean values $x(n)_{\text{rms}}$ of a signal:

$$CF = \frac{\|x(n)\|_{\max}}{x(n)_{rms}} \tag{1}$$

In literature one more parameter can be found - the Peak to Average Power Ratio (PAPR), which is the squared value of CF:

$$PAPR_{dB} = 10\log_{10}\frac{\|x(n)\|^2_{\max}}{x^2_{rms}} \tag{2}$$

The PA operates in the linear region whenever PAPR value of a waveform present at PA input is reduced. The one of the goals when implementing some CFR technique is to minimize in-band and out-of-band distortions. Unfortunately, signal distortion cannot be completely avoided. To quantify the performance of CF reduction operations, the distortion is measured by Error Vector Magnitude (EVM) for in-band and Adjacent Channel Power Ratio (ACPR) for out-of-band signal distortion. [2]

B. PA linearization by DPD

DPD computes the inverse function of the PA transfer characteristic. Utilization of DPD provides PA linearity and high energy efficiency. [1]

We have implemented the DPD solution which models the behavior of PA using complex-valued memory polynomials (MP). The MP model takes into account both PA nonlinearity and memory effects and represents the simplified structure of the Volterra series [2].

The predistorter is positioned in the base-band (BB), before the digital-to-analogue (DA) conversion and BB to RF frequency up-conversion are done. The input signal *x(n)* is processed by DPD block which produces the output signal *y(n)* according the following equation:

$$y(n) = \sum_{i=0}^{N}\sum_{j=0}^{M} w_{ij}\cdot x(n-i)\cdot e(n-i)^j \tag{3}$$

where w_{ij} are complex valued model coefficients:

$$w_{ij} = a_{ij} + \mathbf{j}b_{ij} \tag{4}$$

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$$e(n) = x_I(n)^2 + x_Q(n)^2 \quad (5)$$

The parameters *N* and *M*, used in Eq. (3), represent memory length and nonlinearity order respectively. The signal *e(n)* is the envelop of the input signal *x(n)*.

The DPD coefficients are found in iterative training process which uses recursive least square (RLS) method and indirect learning architecture. The detailed description of DPD method and its implementation in SDR hardware is described in detail in [6].

C. Peak Windowing Method

The Hard Clipping (HC) is conventional CFR approach to constrain signal peaks which exceed selected threshold. The operation of HC is described by Eqs. (6) and (7):

$$y(n) = c(n)x(n), \quad (6)$$

where *x(n)* is the input signal, *y(n)* is the signal obtained after clipping operation is performed. The signal *c(n)* is the clipping function:

$$c(n) = \begin{cases} 1, |x(n)| \le A \\ \dfrac{A}{|x(n)|}, |x(n)| > A \end{cases}, \quad (7)$$

where the parameter *A* is clipping threshold. *x(n)* and *y(n)* are complex signals consisting of quadrature signal components. The HC operation has disadvantage in introducing sharp edges in output signal which increases out-of-band distortion.

In PW method the large signal peaks of input signal are multiplied with a windowing function to smooth the sharp signal edges at clipping points, thus minimizing in-band and out-of-band signal distortion. This not only improves the ACPR of the resulting signal but also limits the peaks to stay under the threshold.

The PW operation replaces the clipping coefficients *c(n)* with new ones *b(n):*

$$b(n) = 1 - \sum_{k=-\infty}^{k=\infty} (1 - c(k))q(n-k), \quad (8)$$

where *q(n)* is a common symmetric window function, for which implementation the Kaiser, Hamming or Hann windowing functions can be used [3, 7].

The calculation of clipping coefficients *b(n)* is implemented by PW FIR filter. Two conditions have to be met. First to ensure that the value of *y(n)* is less than the threshold *A*, the condition given by Eq. (9) must be met:

$$b(n) \le c(n) \quad (9)$$

Besides, to minimize in-band signal distortion the last inequality must be near the equality as much as possible. [3] This implies that narrow window lengths should be used for PW FIR filter implementation.

If clipping rate is too large or wide window length is selected, the adjacent windows in *b(n)* overlap more often, reducing *b(n)*, which yields to more attenuation of the CFR output signal *y(n)*.

The detailed description of PW operation and its implementation in SDR hardware is described in detail in [8].

III. IMPLEMENTATION RESULTS

A. Hardware implementation

The SDR board [9] utilizes two transceiver LMS7002M [10] ICs for frequency conversion between base band (BB) and radio frequencies (RF) and an Altera Cyclone V FPGA, which are used for implementation of DPD and CFR digital blocks. The board is connected to CPU core through high-speed PCIe interface. For the development or demo, test waveform can be uploaded and played from WFM RAM Block, implemented using Altera Cyclone V FPGA resources. In real applications, the CPU Core performs BB digital modem functions, LTE for example. Through PCIe interface the real waveform is fed directly to the CFR block input [10].

The SDR board implements 2x2 Multiple-Input and Multiple-Output (MIMO). It has two transmit TX and two receive RX channels. One spare RX chain is used as DPD monitoring path. In each TX channel, beside DPD and CFR blocks, a low-pass FIR filter is used. The CFR output is filtered by low- pass FIR filter, reducing out of band spectrum regrowth.

PC/GUI implements graphical display for demo and debugging purposes. GUI is capable to show important signals at CFR and DPD block input and outputs in FFT (frequency), time and constellation (I vs. Q) domains.

The board uses LMS7002M on-chip DACs/ADCs [10]. On chip data converters are 12-bit devices. The CFR digital block is implemented as 40-tap FIR filter and operates at 30.72 MS/s sample rate. The CFR block has provision for changing FIR filter order in the range from 1 to 40. Using the same interface, the clipping threshold can be changed up to the signal amplitude maximum level.

The DPD operates at sample rate of 61.44 MS/s. In DPD implementation, the memory length *N*=4 and nonlinearity order *M*=2 are selected.

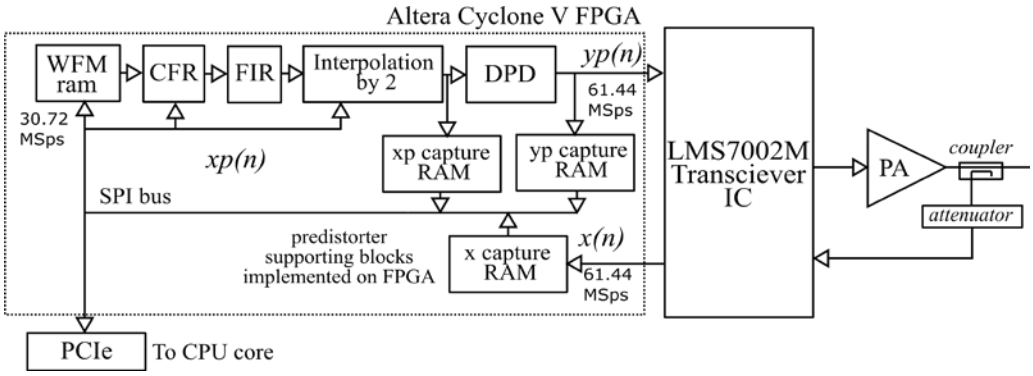

Fig. 1. The CFR and DPD implementation based on SDR transceiver board

The SDR board, together with two 40 dBm Band13 10W power amplifiers have been incorporated in a Personal Computer (PC) based 2x2MIMO base station (BS). To provide power supply to PAs, additional DC/DC converters are incorporated in the BS case. The DC/DC converters get 12V from PC power supply unit and provide 28V, necessary for PA operation.

B. Software implementation

The DC/DC converters and PAs are embedded into base station and these blocks have special input enable pins which are used for external control. We implemented that the DC/DC converters and PAs are controlled directly by SDR board output pins and specially created software application, which is started from Linux command line prompt.

The application provides following commands:

- *startDCDC* and *stopDCDC* to start and stop the DC/DC, and
- *startPA* and *stopPA for* PA turn on and turn off.

Since two independent transmitting channels exist in BS, the commands take as argument constant values 1 or 2 selecting different transmitter channels and corresponding DC/DC and PA.

The same application provides software routines are used for full DPD and CFR control. They are described below.

CFR block is controlled by *setupCFR* command providing different CFR options and parameters. For channel selection there are two options: 1 or 2. The second argument of the *setupCFR* function is the bypass option. Namely, the CFR block can be bypassed by setting the bypass option to 1; otherwise, when CFR is used, this option should be set to zero value. The third argument is CFR FIR filter order, which is an integer value and can be chosen in range from 1 to 40; the last argument is the threshold, specified by positive real number which is less than value of 1.0.

The DPD operation is controlled by several commands which can be generally divided into following groups:

- commands for DPD parameter specification
- starting and stopping the DPD operation
- calibration and reset
- storing and reading the DPD parameters, as well as the DPD coefficients

The DPD parameters are specified by *setGainDPD*, *setLambdaDPD* and *setND_DPD* commands.

The *setGainDPD* is sets the digital gain *Gain* of DPD, adjusting the PA output power when DPD is in training process. The PA output power can be increased, decreased or set to the same level compared to the case when DPD is bypassed. The digital gain is positive real number which can be chosen in range from 0.33 to 6.0.

The command *setLambdaDPD* specifies the DPD "forgetting factor" λ which adjusts the speed of DPD algorithm convergence, e.g. how fast the PA becomes linearized. The λ is the real positive number close to one.

Command *setND_DPD* defines the DPD delay line length *ND*.

The command *calibrateDPD* automatically performs DPD parameter calibration. It calculates the DPD delay line length *ND* and gain value *Gain*. When DPD training process is started, the PA output signal power remains at the same level as in case when DPD is just bypassed. Without any loss in output power, the PA becomes linearized when DPD is calibrated and then, training process is started.

Command *resetDPD* is used for DPD coefficients reset operation. When DPD coefficients are reset, it is identical situation as when DPD is bypassed.

The commands *saveConfigDPD* and *loadConfigDPD* store into the memory and read from memory the last found DPD parameters *ND*, *Gain* and λ.

The operation of DPD training is started and stopped using *startDPD* and *stopDPD* commands respectively. It is strongly recommended that DPD is calibrated before it is started. When DPD is started, the DPD filter coefficients are continuously changed in the DPD training process.

Commands *loadCoeffDPD* and *saveCoeffDPD* store and read from memory the DPD filter coefficients. Using these commands the PA can be compensated when the DPD coefficients are just read from memory and loaded into FPGA, even when DPD training operation is not

started by *startDPD*.

All software routines are written in C++.

C. Measurement Results, case of 10MHz LTE waveform and 10W PA

The CFR and DPD methods were implemented in SDR board FPGA IC to reduce the distortions of transmitted signals observer at PA output The SDR board has been incorporated into PC-based BS, together with two RF PAs having 10W modulated output power. The PAs have following characteristics: the bandwidth is 700-850 MHz; average output power at 1 dB compression point is 40 dBm at the frequency of 750 MHz.

The amount of out-of-band and in-band distortion is measured in terms of ACPR and EVM respectively. |Here, the results are provided for 10MHz LTE waveform. In the measurements different CFR parameters are considered. For example, the filter order is changed in following steps L=9, 19, 29 and 39. Also, different clipping thresholds are evaluated, staring from Th=1.0 down to Th=0.6. While these parameters are changed, the level of transmitted output power is kept at the same level as before linearization process is started.

The measured PAPR of original waveform, when DPD and CFR are bypassed, is PAPR= 10.3 dBm. The measured EVM in this case is EVM=1.26 %. When CFR and DPD are utilized, the EVM is worsened when threshold *Th* value is reduced, and also when the CFR filter order L is increased. For example, in case of L=39 and Th=0.6, the EVM =7.81%.

At starting point, when neither CFR nor DPD are utilized, the ACPR=-37.5 dBc and EVM=3.32%. The measured PA output power is Pout=39.7 dBm.

The distortion is removed by DPD and CFR. The ACPR is decreased from starting value of -49.6 dBc, obtained for threshold Th=1.0 to the minimum value equal to -50.8 dBc, obtained at Th=0.6. The power of PA output signal is maintained at the same level as at starting point, before any CFR and DPD data processing is done.

When PAPR is decreased by 2dB (from PAPR=10.3 dB down to PAPR=8.3 dB), for L=19 and Th=0.76, the EVM=2.42%, ACPR=-50.5dBc. Therefore, the ACPR is improved by 13 dBc and EVM by 0.8%.

IV. CONCLUSION

CFR and DPD algorithms have been implemented on SDR board and verified by measured results. When DPD is used without CFR, the modulated signal power at PA output needs to be backed-off for approximately 2 dB to enable DPD to remove distortions down to the system noise floor. When CFR is utilized, DPD is capable of cancelling any out-of-band distortion above system noise floor, without PA power back-off.

The DPD and CFR are controlled by specially created software application which is started through Linux command line prompt. The application provides full DPD and CFR control.

The main characteristics of our solution are low implementation complexity and good performance measured in terms of EVM and ACPR as key parameters.

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