Radiation impact modelling method for gate level design verification

Artur Petrosyan

Abstract – A radiation impact modelling method is presented in this paper. The method is aimed to be used in gate level design verification. A software tool was designed based on the method to configure the radiation impact parameters and automatically inject the radiation-induced single event upset and single event transient effects in the synthesized gate-level netlist. The work aims to provide a new method to speed up the design process of radiation-hardened digital integrated circuits. Experimental results of the proposed method show accuracy loss about 3-4% and simulation speed-up by 2-3 times compared to existing methods. The proposed method effectively verifies the design resistance to radiation impact.

Keywords - Single event upset (SEU), Single event transient (SET), Radiation impact (RI), Synthesis, Radiation modelling.

I. Introduction

Radiation impact (RI) on integrated circuits (IC) forms effects such as single event transient (SET) and single event upset (SEU) which lead to failures (soft errors) in the combinational and sequential parts of ICs. It is known that there are three general masking factors (logical, electrical and timing) which may filter out the influence of the SET or SEU effect [1]. The influence is logically masked (filtered) when one of the inputs of the logic gate is the dominant, the influence is electrically masked when the RI does not form enough energy to assert a SET or SEU, and the RI is timing masked if the SET occurs when there is no latching window for the memory elements [2]. However, these masking factors do not grant that the IC will work without failures.

Testing and verification of the ICs with consideration of discussed effects is becoming more important as the safety requirements for ICs used in automotive systems and other spheres are getting higher [3], [4], [5].

Different RI models have been proposed so far. The methods proposed in [6] uses device-level simulations to analyse the RI. As an alternative to the device level simulations, the method proposed in [7] uses a double exponential current pulse in circuit-level simulators for modelling the RI. However, these modelling techniques of RI have poor performance when they are applied to large designs. The technique proposed in [8] partly solves the performance of RI modelling in large designs. This method uses Verilog gate level models to modify the entire logic cell library to characterize the Multiple-Event-Transient (MET) in gate level simulation. The main disadvantages of the method are time-consumption and inefficient insertion of MET effects in all the cells in the library, as, the probability of RI occurrence on all the cells in design is low [9]. Another disadvantage of this method is that it considers simulations of only SET effects.

Thus, new methods are needed in gate level simulations to speed-up the RI simulations and model not only the SETs but also the SEUs.

Artur Petrosyan is with Synopsys Armenia Educational Department Synopsys Armenia CJSC, 41 Arshakunyats Ave, Yerevan, Armenia, E-mail: arturp@synopsys.com

II. SET and SEU gate level models

The SET and SEU radiation effects are random in nature therefore these effects occur at unpredictable moments on random locations [4]. Two Verilog models are suggested for gate level simulation. The models consider the randomness of the effects.

A. SET model

The model (Fig. 1) contains a random pulse generator, a random number generator, logic to randomly select a cell, and an XOR gate.

The random pulse generator is used for generating *N* number of pulses during a period to make the occurrence of SET random. The other random number generator is used to make the pulse widths of the SET random. To apply the generated pulse (SET effect), a cell is selected from the gate level netlist. The output of the cell and the pulse signal are connected to the XOR gate. If the SETs propagate through combinational circuits with influence of masking factors no failures will be detected.

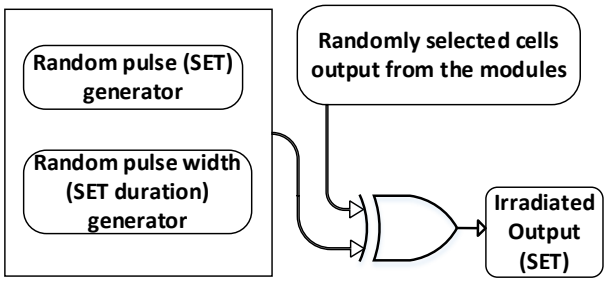

Fig. 1. Block diagram of the SET model

B. SEU model

To make verification process more controllable and make sure that masking factors don't affect error injection

process, a model is suggested to test only sequential circuits by inserting SEU directly on the outputs of elements. The Verilog model (Fig. 2) uses an inverter to flip the state of sequential element. The inverter is connected to the output "Q" port.

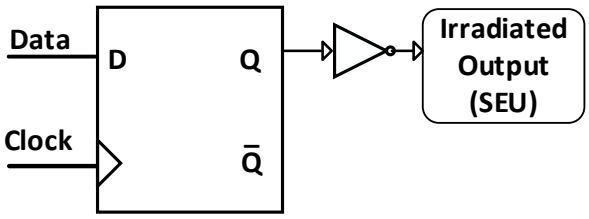

Fig. 2. Block diagram of the SEU model

III. THE PROPOSED METHOD FOR RADIATION MODELLING IN GATE LEVEL SIMULATION

A general overview of the proposed method is shown in the flowchart (Fig. 3), where the first step is the logic synthesis of the RTL design. After this step, the gate-level (synthesized) netlist is generated. The generated netlist is then simulated to save the waveforms as golden results for further comparison and estimation of the RI.

The next step is finding the module and cell instances by passing through the gate-level netlist. The information such as module and cell instances are saved in vectors. For example, module instances are saved in modules vector Eq. (1) and the cell instances are stored in cells vector Eq. (2).

$$M = (m_1, m_2, .., m_i) \quad (1)$$

$$C = (c_1, c_2, .., c_i) \quad (2)$$

where i is the number of the cell or module instances in the given netlist.

In gate-level netlists, the module instances contain cells. Thus, the cell vectors are related to the modules. Each module instance vector consists of cell instances vector Eqs. (3), (4) and (5).

$$m_1 = C_1(c_1, c_2, .., c_i) \quad (3)$$

$$m_2 = C_2(c_1, c_2, .., c_i) \quad (4)$$

$$m_n = C_n(c_1, c_2, .., c_i) \quad (5)$$

where n - is the amount of the logic cells in each module instance.

The fourth step is calculating the probability of RI occurrence in a design. This allows modelling the unpredictable RI behaviour (discussed in previous section) and to avoid applying the RI effects on all the cells in the design.

The probability is calculated using exponential density function Eq. (6) [10], [11] for each module in module instances vector and for each cell in cell instances vector.

$$p(t) = \frac{1}{\tau} e^{-t/\tau} \qquad F(t) = \int_0^t p(t)dt = 1 - e^{-t/\tau} \quad (6)$$

where t – is the SEU or SET assertion period τ – is the time after the assertion of the effects.

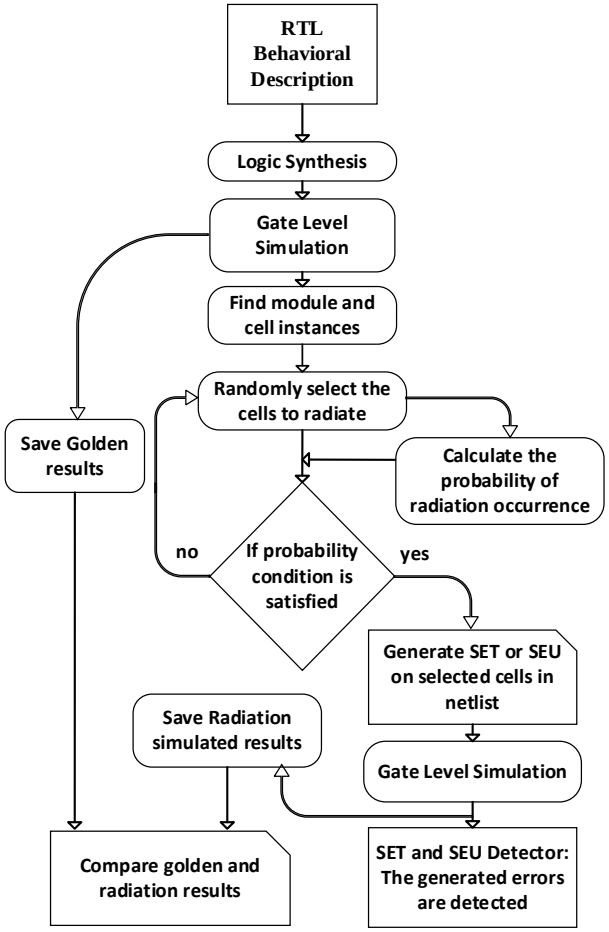

Fig. 3. General overview of the radiation effect (SET, SEU) modelling method

The fifth step is the generation of the SET or SEU effects on module and cell instances vectors.

From the module instance lists the highest RI probability elements are randomly selected. Then based on the type of the instances (combinational or sequential) the SET or SEU (Figs. 1 and 2) models are applied. In order to apply the effects, the selected cell is replaced in the gate level netlist with a modified (radiation effect injected) model.

Next, the gate level simulation of the modified netlist is performed to save the radiation simulated waveforms. During the simulation, the detected errors are extracted using SET and SEU error extractor (Fig. 4).

The error detection and extraction are developed for further error analysis. It is implemented by a separately

generated Verilog module for the gate-level netlist. This module counts errors on each SET or SEU occurrence. It also detects the time/moment of each error and extracts its value to help to debug and analyse the results (Table I).

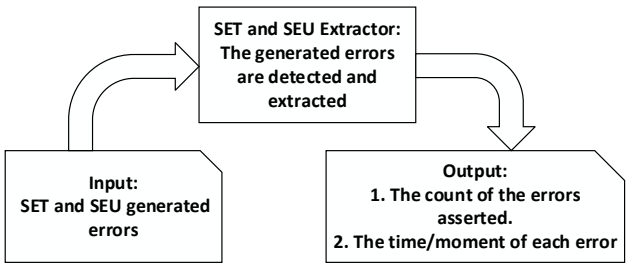

Fig. 4. Block diagram of radiation effect (SET or SEU) extractor

Result analyses are performed by comparing the saved golden simulation waveforms of the gate-level netlist without taking into account RI and the simulation waveforms with consideration of RI on the generated netlist.

IV. Experimental Results

The proposed method was implemented as a software tool in the digital design flow. The tool automates the proposed method (Fig. 3) and allows configuration of the RI parameters. A number of ISCAS89 benchmark circuits [12] were implemented in Verilog and tested using VCS environment [13] to determine the error rates and perform design modification to protect it against RI.

To generate the gate-level netlist synthesis of the s27 benchmark circuits was done using Synopsys Design Compiler [14] in SAED32nm technology [15].

The VCS simulation waveform results of synthesized netlist are saved as golden results (Fig. 5).

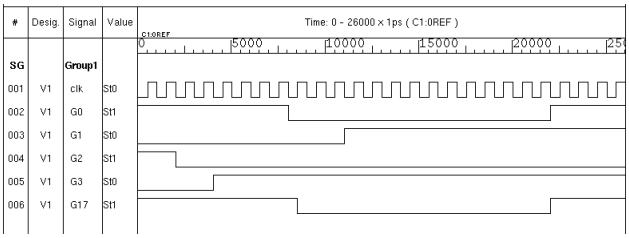

Fig. 5. VCS simulation results of ISCAS89 S27 benchmark circuit without RI as golden results

The synthesized netlist is then used to apply modification to inject SET or SEU using the RI models (Figs. 1 and 2) and the proposed method (Fig. 3). The VCS simulation waveform with RI models is saved (Fig. 6) and errors are extracted (Table I) using the SET (or SET and SEU) error extractor module.

The highlighted signals in Fig. 6 indicate the error which occurred on the output of s27 benchmark circuit with clock capturing edge.

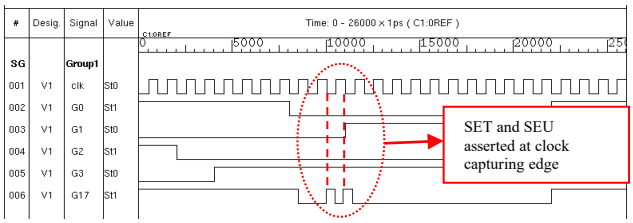

Fig. 6. VCS simulation results of ISCAS89 S27 benchmark circuit with RI

TABLE I
Detected errors for ISCAS89 s27 benchmark circuit

Cell Type	RI Type	RI Period(*ps*)	Total RI error count	Total RI reached output
NAND	SET	9958-10434	14	2
NOR	SET	9958-10434		
DFF	SEU	10862-11386		

The result analysis by comparing the golden and modified gate-level netlist waveforms is performed using Synopsys Verdi tool [16]. This tool shows all the differences between the golden and irradiated simulations and allows to debug the design.

A waveform comparison result (Fig. 7) of the ISCAS89 s27 benchmark circuit is done. Signals from the golden waveform are compared to the corresponding signal in the irradiated waveform. The DFF state change is detected on the clock falling edge when the RI occurred. Without the RI the DFF stores logic '1'. However, instead of the logic '1' a logic '0' appears at the output of the DFF cell. Which results in SET propagation through the entire design to its output.

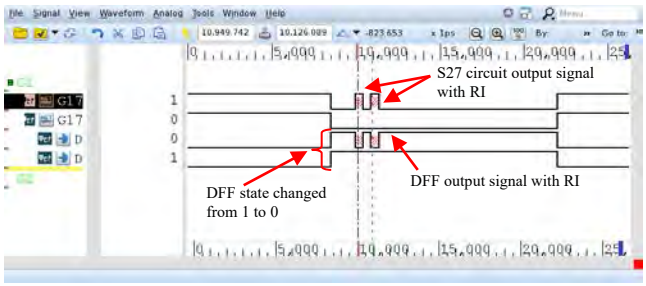

Fig. 7. The comparison results of S27 benchmark circuit with RI and without RI

To verify the proposed method several benchmark circuits from ISCAS89 series were simulated. The same benchmarking circuits are tested with HSPICE simulator [17] and the MET simulation method proposed in [8]. The simulation results show that the accuracy of the proposed

method is 3-4% less compared to the HSPICE simulations due to electrical masking factors but it is similar compared to MET simulation method.

From the other hand, the results of CPU runtime (Table III) show that simulation time of the circuits is about 2-3 times faster using the proposed methodology.

TABLE II
COMPARISON RESULTS OF THE PROPOSED METHOD ACCURACY FOR THE ISCAS89 BENCHMARK CIRCUITS COMPARED TO EXISTING METHODS

ISCAS89 circuits	Total RI error count	Total RI reached output		
		HSPICE [17]	MET simulation method [8]	Proposed method
s27	14	3	2	2
s298	28	14	13	12
s344	132	54	50	52
s953	675	86	76	82

TABLE III
SIMULATION RUNTIME COMPARISON RESULTS FOR THE ISCAS89 BENCHMARK CIRCUITS

ISCAS89 circuits	Total RI error count	HSPICE [17] CPU(Sec)	MET simulation method [8] CPU (Sec)	Proposed method CPU (Sec)
s27	14	22,8	7,35	4,15
s298	28	28,4	15,23	6,4
s344	132	52,36	28,9	10,45
s953	675	73,22	35,7	15,35

V. CONCLUSION

The radiation impact modelling and simulation method in gate level design verification is presented. The method was automated as a software tool and tested using the ISCAS89 benchmark circuits. The experimental results show that the runtime of the simulations of digital circuits considering radiation impact is reduced about 2-3 times while the accuracy loss is about 3-4%. The results prove that the proposed method can be integrated into the digital circuit design process for gate level design verification.

REFERENCES

[1] Mariem Slimani, Lirida Naviner, "A tool for transient fault analysis in combinational circuits", 2015 *IEEE International Conference on Electronics, Circuits, and Systems (ICECS),* pp. 125 - 128, Dec. 2015.

[2] P. Shivakumar, M. Kistler, S.W. Keckler, D. Burger, L. Alvisi, "Modeling the effect of technology trends on the soft error rate of combinational logic", *Proceedings International Conference on Dependable Systems and Networks*, pp. 427-430, June 2002.

[3] Vazgen Melikyan, "Simulation and Optimization of Digital Circuits", *Springer International Publishing,* pp. 10-77, Jan. 2018.

[4] Ghaith Bany Hamad, Syed Rafay Hasan, Otmane Ait Mohamed, "Modeling, analyzing, and abstracting single event transient propagation at gate level", *2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 515-518, Aug. 2014.

[5] Fei Gong, Meenal Vaidya, Rishvanth Kora, Daniel Harshbarger, "A FPGA based prototype verification in automotive mixed signal integrated circuit development", *2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1200-1203, Dec. 2013.

[6] Paul E. Dodd, "Physics-based simulation of single-event effects", *IEEE Transactions on Device and Materials Reliability,* Vol. 5, No. 3, pp. 515-518, Sept. 2005.

[7] William G. Bennett, Nicholas C. Hooten, "Experimental Characterization of Radiation-Induced Charge Sharing", *IEEE Transactions on Nuclear Science,* Vol. 60, No. 6, pp. 4159 - 4165, Dec. 2013.

[8] Akira Mochizuki, Naoya Onizawa, Akira Tamakoshi, Takahiro Hanyu, "Multiple-event-transient soft-error gate-level simulator for harsh radiation environments", *TENCON 2015 - 2015 IEEE Region 10 Conference,* Vol. 60, No. 6, pp. 978 - 983, Jan. 2016.

[9] T. Rejimon, S. Bhanja, "A Timing-Aware Probabilistic Model for Single-Event-Upset Analysis", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 14, No. 10, pp. 1130 - 1139, Oct. 2006.

[10] Grecki, Mariusz, "VHDL Simulation considering Single Event Upsets (SEUs)", *Technical Proceedings of the 2006 NSTI Nanotechnology Conference and Trade Show*, pp. 717 - 720, Jan. 2006.

[11] Marta Bagatin, Simone Gerardin, Alessandro Paccagnella, "Single Event Upsets Induced by Direct Ionization from Low-Energy Protons in Floating Gate Cells", *IEEE Transactions on Nuclear Science,* Vol. 64, No. 1, pp. 464 - 470, Dec. 2017.

[12] E. Brglez. D. Bryan, K. Kouninski., "Combinational profiles of sequential benchmark circuits" ISCAS89 Proceedings", *ISCAS89 Proceedings*, pp. 124 - 198, Dec. 1989.

[13] VCS® User Guide, *Synopsys Inc*. – 2019. pp. 56-254

[14] Design Compiler User Guide, *Synopsys Inc.* – 2019. pp. 138-175

[15] R. Goldman, K. Bartleson, T. Wood, K. Kranen, C. Cao, V. Melikyan, G. Markosyan, "Synopsys' open educational design kit: Capabilities, deployment and future", *2009 IEEE International Conference on Microelectronic Systems Education*, pp. 20 - 24, Sep. 2009.

[16] Verdi® SystemC Debug User Guide, *Synopsys Inc.* – 2017. pp. 24-76.

[17] HSPICE Application Manual, *Synopsys Inc*., 2018. pp. 617-712.