SPICE simulation of memristor logic functions

Luka Spahić, Miljana Milić

Abstract - In this paper, the short review of memristor models applicable for logic operations is given. Further, this paper describes elementary logical functions such as AND, OR and NOT and the application of the developped memristor model for their realization. Logical functions are verified in PSPICE.

Keywords – Memristor, simulation, logic functions, modelling.

I. Introduction

Currently, we know and we are using three basic circuit elements: a resistor, a capacitor and an inductor. But, in the 1971., the missing fourth element has been proposed by L. Chua [1]. Memristor is a two-terminal circuit element that links electric charge and magnetic flux, and later shows a resistive switching characteristics. Its state is definded by a time integral of current and a time integral of voltage.

At the time when Chua was theoretically proposing the idea of a memristor, it hasn't yet practically been manufactured. Finally, in 2008. R. Stanley William and his team, at HP Labs, made a discovery of the first physical memristor. This memristor was based on TiO_2 material doped with oxygen vacancies and had resistive switching characteristics. They have used a TiO_2 material placed between two platinum (Pt) electrodes, with one of the regions doped with oxygen vacancy (TiO_{2-x}) as shown in Fig. 1. The doped region, marked as *w*, has a lower resistivity than the undoped region. When applying a certain voltage across the element, the doped region will expand or shrink which will result in a resistance change.

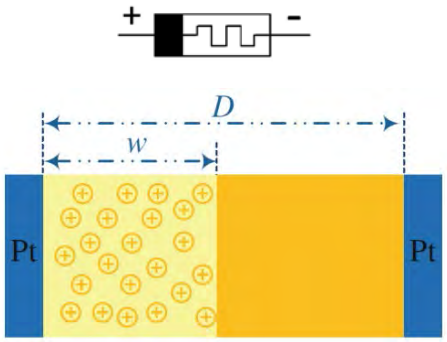

Fig. 1. HP memristor TiO_2 structure [3]

Luka Spahić and Miljana Milić are with the Faculty of Electronic Engineering, University of Niš, Aleksandra Medvedeva 14, 18000 Niš, Serbia.
E-mail: luka.spahic@elfak.rs, miljana.milic@elfak.ni.ac.rs

When the voltage is revoked, the states of the oxygen vacancy carriers remain unchanged, and that is why the device can "memorize" its previuse resistance value [2].

Since 2008, many researchers were trying to make a suitable model of memristor that could be used in future applications. The greatest advantage of the memristors is that they are extremely small as compared to the size of MOS transistors. In fact, a memristor can be manufactured with area as small as 9 nm^2 [4]. Due to their ability to memorize previuse states, memristors could be used for non-volatile resistive memory systems (ReRAM) and also because of their extremely small size, they could be very conveniently built in a crossbar array.

Several papers have been published with the description of memristors possible application in the implementation of logic functions. This will also be the subject of this paper. Down below, common design styles are briefly described.

Most common memristor logic models are IMPLY logic and MAGIC design. In IMPLY logic [5], memristors can be used to realize implication operation such as $p \rightarrow q = p' + q$. The initial values of p and q, and also the result are "stored" as resistance values in memristors. Here we are using two voltages for the initialization, but MAGIC uses only one.

In MAGIC memristor design style [6], memristors are used to implement logic functions/gates, where the inputs are applied as values of resistance. This also applies for the output values.

In this paper, two memristor SPICE models are reviewed. The first one, is a memristor model presented by HP (but SPICE description is given by Biolek [7]), which is considered to be the most efficient. But on the other hand, this model can properly operate for very low frequencies (1 Hz – 5 Hz). The second one, is an improved model [8] with ability to operate on frequencies between 1 kHz – 10 kHz. Next, the SPICE simulations that shows usage of new improved memristor model as type of logic function (OR, AND, NOT) are given in section III. Through out section III simulation results are discussed.
Finally, we have come to conclusion of further reaserch of memristors based on discussion in section III.

II. Review of Memristors Logic Models

As previously mentioned, we have encountered two memristors models and one of them has been used for further simulations.

A. SPICE Model of Memristor with Nonlinear Dopant Drift[7]

The electric circuit of the first SPICE model is given in figure 2. To model the relation between voltage and current the following expression could be applied:

$$R_{MEM}(x) = R_{OFF} - x\Delta R, \Delta R = R_{OFF} - R_{ON} \quad (1)$$

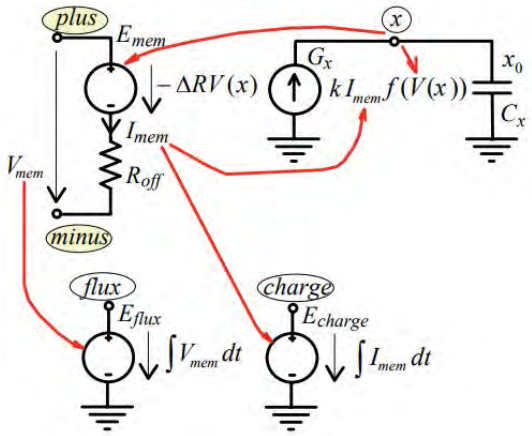

Fig. 2. Electric circuit of SPICE model [7]

As shown in fig. 2, eq. (1) corresponds to R_{OFF} resistor which is in series with E_{MEM} whose terminals are controlled according to eq. "- ΔRx". The width x of the doped layer is modeled by the voltage V (x) of the capacitor C_X. The initial state of the normalized width x of the doped layer x_0, modeld by initial capacitor voltage which depends of the initial resistence R_{INIT} according to formula (1) [7]:

$$X_0 = \frac{R_{OFF} - R_{INIT}}{\Delta R} \quad (2)$$

The memristor library function for this model is as follows:

```
* HP Memristor SPICE Model * For Transient Analysis only *
+created by Zdenek and Dalibor Biolek
**************************
* Ron, Roff - Resistance in ON / OFF States
* Rinit - Resistance at T=0
* D - Width of the thin film
* uv - Migration coefficient
* p - Parameter of the WINDOW-function
* for modeling nonlinear boundary conditions
* x - W/D Ratio, W is the actual width
* of the doped area (from 0 to D) *
.SUBCKT memristor Plus Minus PARAMS:
+ Ron=1K Roff=100K Rinit=80K D=10N uv=10F p=1
*********************************************** *
DIFFERENTIAL EQUATION MODELING *
***********************************************
Gx 0 x value={ I(Emem)*uv*Ron/D^2*f(V(x),p)}
Cx x 0 1 IC={(Roff-Rinit)/(Roff-Ron)}
Raux x 0 1T
* RESISTIVE PORT OF THE MEMRISTOR *
*******************************
Emem plus aux value={-I(Emem)*V(x)*(Roff-Ron)}
Roff aux minus {Roff}
***********************************************
*Flux computation*
***********************************************
Eflux flux 0 value={SDT(V(plus,minus))}
***********************************************
*Charge computation*
***********************************************
Echarge charge 0 value={SDT(I(Emem))}
***********************************************
* WINDOW FUNCTIONS *
* FOR NONLINEAR DRIFT MODELING *
***********************************************
*window function, according to Joglekar
.func f(x,p)={1-(2*x-1)^(2*p)}
*proposed window function
.func f(x,i,p)={1-(x-stp(-i))^(2*p)}
.ENDS memristor
```

As can be shown in mentioned paper [7], described model above can not be used for frequencies higher than 5 Hz. This also, has been proved in paper [8], and that's why we have choose a new model which is based on Biolek model, but improved for higher frequencies.

B. A new improved model

This model is based on a Biolek SPICE model mentiond before and it represents an improvement in frequency domain. An improved electric circuit of the model [8] is shown in figure 3. After that, a SPICE model that describes circuit in Fig. 3 is given.

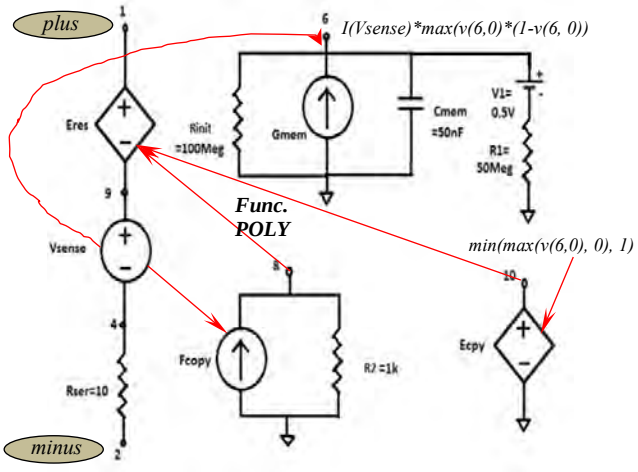

Fig. 3. New memristor model [8]

Here, POLY function that can directly calculate the value of integration is used instead of a regular integration function. A small value of R_{SER} is resistance used for current sensing between terminals 1 and 2. A clamping

circuit is used to initiate the operation of the memristor. Both, charge and flux depend on the state of the memristor, sensed at node six. The memristor terminals 1 and 2 are marked with red circles.
The used sub circuit PSPICE description is given next:

```
.SUBCKT newmem 1 2
*****************************
**Squared quantity of voltage**
Eres 1 9 POLY(2) (8, 0) (10, 0) 0 0 0 0 1
*****************************
Vsense 9 4 DC 0V
*****************************
**Current sensing**
Fcopy 0 8 Vsense 1
R2 8 0 1k
Rser 2 4 10
**Differential equation**
Gmem 6 0 VALUE={I(Vsense)*max(v(6,0)*(1-v(6, 0)), +0)}
Cmem 6 0 50nF
*****************************
**Limiting the window of 0 and 1**
Ecpy 10 0 VALUE={min(max(v(6,0), 0), 1)}
*****************************
Rinit 6 0 100Meg
V1 6 7 DC 0.5V
R1 7 0 50Meg
.ENDS newmem
```

It can be noticed, that the new model doesn't have parametric structure. So, the values of D i.e., width of the thin film, and u_V – migration coefficient, etc., remain unknown. Figure 4 represents a well known I-V characteristic of memristor by HP [2]. The I-V characteristic of new model used in this paper is shown in Fig. 5.

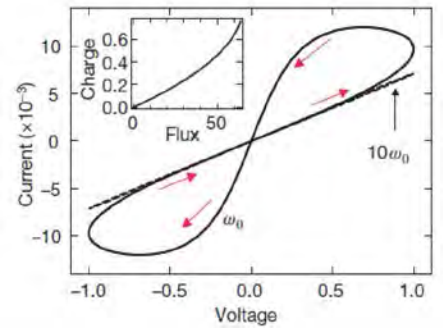

Fig. 4. Memrisor I-V characteristic [2]

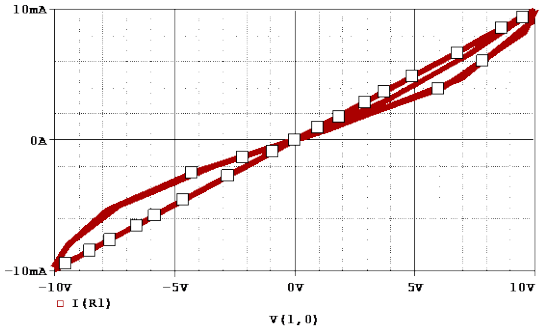

Fig. 5. A hysteresis curve on application of a sinusoidal signal 10V, 5kHz. The I-V characteristics of the memristor obtained by SPICE simulation

Further in the paper, authors will describe simulation results and memristors based realizationa of AND, OR and NOT logical functions.

III. Simulation Results

Our simulations did not use MAGIC or IMPLY design. Instead, we have applied the input voltage [0 V, 5 V] while observing currents and voltages accros particular memristors. This was done only for AND and OR logical circuit. For NOT logic function, it was necesary to apply excitation voltage V_O, in order to obtain voltage accros input memristor and output memristor.

In oder to simulate AND, OR and NOT logical functions, memristors have to be connected in a certain way as given in figure 6.

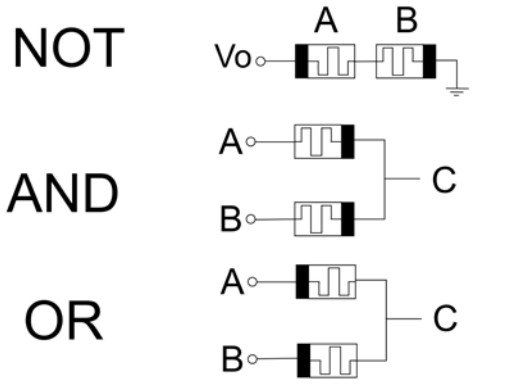

Fig. 6. Realised basic logic functions using memristors

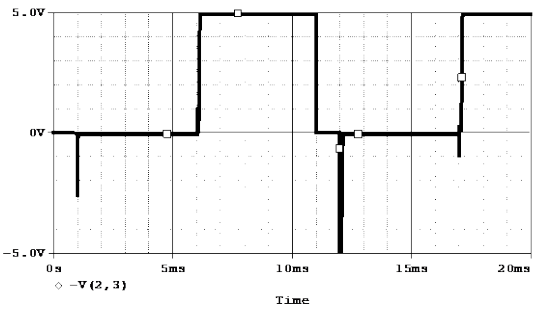

Fig. 7. Voltage accros memristor A of an inverter

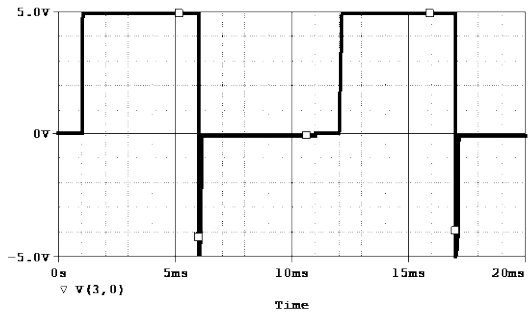

Fig. 8. Voltage accros memristor B for an inverter

For the simulation of an invertor, V_O voltage was applied. By applying V_O, resistances of memristor A and B was changing. According to that change, we can see that voltage accros memristor A represents inverted voltage of the memristor B. This confirms the assumptions that this circuit has properties of an invertor.

Signals of the memristors A and B are shown in Figures 7 and 8, respectively.

The AND and OR gate, there is no need for the V_O voltage. Simulations show that when logical "0" and "1" are applied at memristor A and B, memristor C gives voltage or current response that describes AND or OR logical function. Signals for AND gate are shown in figure 9, where red color relates to signal A and blue color relates to signal B. Green color represents the voltage of the output signal.

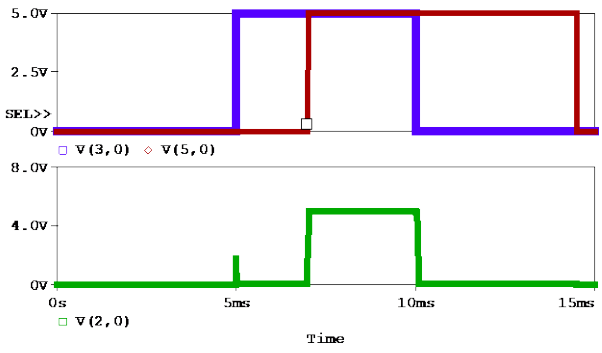

Fig. 9. Signals for AND gate

Signals for OR logic function are shown in figure 10, where red color coresponds to the voltage accros memristor A, while blue color corresponds to voltage accros memristor B. Green color represents the output signal voltage. As one can see from these waveforms, the output voltage, represents the OR logical function for A and B input combinations. The hazardous behavior of the voltage drop happens with transition of inputs high to low voltage level, when output drops to 0 V and after goes to 5V. This glitch represents an unwanted behavior and it can cause various readout errors.

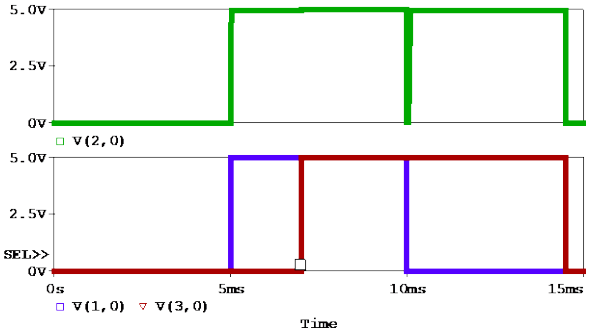

Fig. 10.Signals for OR gate

IV. Conclusion

The simulation of memristor logic model implemented in the software OrCad Pspice shows results relevant to the original logical AND, NOT and OR functons. The chosen way of simulation was the easiest to understand and to simulate.

Also, different SPICE memristor models are described. The first model is the most efficient, but it only works for very low frequencies which in digital electronics has no practical use. The second model, shows that with some changes in model design, it can work on higher frequiencies which is an andvatige, but with current technology it is still a simulation model.

Using memristors as logic gates would decrease power consumption and because of their nano scale structure thay could decrease or replace usage of traditional components such as CMOS transistors in logic gates. Further reaserch would be oriented into the elemenation of unwanted glitches. The increase of its speed should bring major advantage to memristor technology for its use in Crossbar arrays. The applications of memristors in RAM could make an important change in the memory storage systems realization.

Acknowledgement

This research was patially funded by The Ministry of Education and Science of Republic of Serbia under contract no. TR32004.

REFERENCES

[1] L. Chua, "Memristor – The missing circuit element," *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507–519, Sep 1971.

[2] D. B. Strukov, G. S. Snider, D. R. Steward, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008.

[3] Radwan, Ahmed G., Fouda, Mohammed E. – On the Mathematical Modeling of Memristor, Memcapacitor, and Meminductor DOI: 10.1007/978-3-319-17491-4

[4] A. Sinha, M. S. Kulkarni, and C. Teuscher, "Evolving nanoscale associative memories with memristors," in Proc. of *11th IEEE Conference on Nanotechnology*, Aug 2011.

[5] S. Kvatinsky, G. Satat, N. Wald, E. G. Friedman, A.Kolodny, and U. C. Weiser, "Memristor-Based Material Implication (IMPLY) Logic: Design Principles and Methodologies," *IEEE Trans. VLSI Syst*., vol. 22, no. 10,pp. 2054–2066, Oct 2014.

[6] S. Kvatinsky, D. Belousov, S. Liman, G. Satat, N. Wald, E. Friedman,A. Kolodny, and U. Weiser, "MAGIC – Memristor-Aided Logic," *IEEE Trans. Circuits Syst. II*, vol. 61, no. 11, pp. 895–899, Nov 2014.

[7] Z. Biolek, D. Biolek, and V. Biolkov´a. "SPICE model of memristor with nonlinear dopant drift." *Radio engineering J.*, 18(2):211, 2009b.

[8] Ketaki Bhave, Dr. Nisha Sarwade "Memristor Modeling Using PSPICE" *Int. Journal of Engineering Research and Applications Vol. 4, July 2014, pp.139-143*