A Graph Perspective on Logic Circuits: Faults, Robustness & Eigenspectrum

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Abstract – Graphs can be used to model logic circuits with vertices denoting nodes of the electrical network and edges representing connections between nodes through a logic gate. Consequently, linear algebra, perturbation and spectral matrix theory provide a framework for exploration of concepts such as circuit robustness, and fault detection and identification. This paper, through a set of benchmark circuits, illustrates how the aforementioned mathematical and engineering concepts are intertwined. In particular, through means of simulation, it was revealed that some of ISCAS'85 circuits exhibit higher robustness to open-circuit faults, but higher ability to locate (fatal) short-circuit faults.

Keywords – Faults, Graph modelling, Circuit Robustness, Spectral Analysis.

I. Introduction

Design of logic circuits (and electrical networks in general) represents a great challenge from the perspective of error-tolerance (robustness), fault detection and testability. Employed design techniques are often highly dependable on the nature of the desired circuit function [1] and require to consider different types of faults simultaneously. This hinders comparison between circuits and measurement/approximation of their robustness. Particularly, in testing of combinational circuits, obstacles emerge such as delay and timing skew effects [2] rendering the definition of (near)-minimal test set a hard problem. Some sophisticated techniques rely on probabilistic approaches to error estimation [3].

Furthermore, use of graph algebraic theory in the analysis and design of electric circuits is a rich discipline that has provided concepts such as the connection between Laplacian matrix eigenvalues and effective resistance [4], and Kron reduction of graphs as a way to analyse an electrical network through a generalization of $Y-\Delta$ transformation [5]. However, perception of circuits' robustness and testing has not been often viewed upon from a graph perspective. Hence, this paper provides an illustration of how some of the related features of combinational logic circuits reflect in (spectral) graph theory.

On several ISCAS'85 benchmark circuits it is shown that the density of graph eigenvalues expresses a circuit's sensitivity to (open/short circuit) faults, *i.e.* that higher distance between eigenvalues makes the circuit more robust. Moreover, the emergence of a dominant eigenvector in a faulty circuit was recognized as potential marker for detection of a fault and its localization.

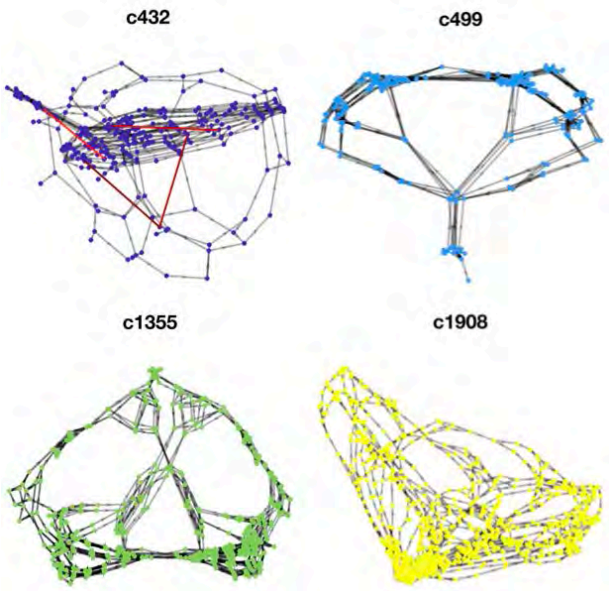

Fig. 1. Graph representation of the benchmark circuits

The main section of the paper consists of three subsections: in the first, the description of benchmark circuits is provided; further, spectral and statistical approach for evaluation of circuits' robustness is presented with the main results reported; and then, a discussion is given on the relationship between the spectral results, and circuits' robustness and identifiability of faults. The conclusion contains a summary of advantages of the graph perspective on circuits' robustness, and the main limitations of the approach in the current form.

II. Graph Spectral Analysis of Circuits

A. Data

The analysis reported in this paper was performed on combinational ISCAS'85 benchmark circuits of different sizes, specifically, c432 (27-channel interrupt controller), c499, c1355 (32-bit single-error-correcting circuits), and c1908 (16-bit single-error-correcting/double-error detecting circuit) [6]. These circuits were collected in the form of

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Verilog descriptions. In order to perform graph-based analysis on the data, Verilog netlists needed to be transformed into appropriate graph representations. This was done with java-based toolbox *Verilog2GEXF*, which was developed as a free and universal visualization tool [7]. For each netlist, the tool exports a graph with n nodes and m edges that can be described as a square adjacency matrix $\mathbf{A}$ of size n with exactly m nonzero entries equal to 1 called edge weights. The graph vertices denote nodes of a logic circuit, whereas edges represent connections between nodes through a logic gate (Fig. 1). Resulting graph gives a simplified model of the electrical network from the perspective of information flow. This is explained in more detail for the toy example circuit in the following subsection.

B. Methods & Results

Graph representation of a logic circuit is given in the form of a binary adjacency matrix, having an entry equal to 1 at position (i, j) if there is a connection between j^{th} and i^{th} node in that direction as seen by the information flow through a logic gate. Fig. 2(a) shows the adjacency matrix of a simple circuit encompassing one AND and one NOT gate (top row). Notice that there is also a connection at the entry $(2,2)$, *i.e.* there is a self-loop edge at the node corresponding to the circuit output. This feature is automatically added by the used toolbox converting Verilog netlists, in order to reflect the notion of accumulation of information at the output, since it cannot flow anywhere from there.

The output of an information flow through the circuit can be modelled as $\mathbf{A}\boldsymbol{x}$, where $\boldsymbol{x}$ is the column vector of the input. Note that this is not the same as the function of the circuit in terms of voltages and currents as in modified nodal analysis. Here, all gates are represented as adders. Moreover, the final output of the simulated flow in the case of the circuit in Fig. 2 is given by $\mathbf{A^2}\boldsymbol{x}$. In general, this corresponds to a vector $\mathbf{A}^{\boldsymbol{l}}\boldsymbol{x}$, where l is the number of gate levels in the hierarchy of the circuit's implementation.

Given a graph described by its adjacency matrix $\mathbf{A}$, the eigendecomposition of the graph/matrix refers to the set of n eigenvectors $\boldsymbol{u_i}$ concatenated into matrix $\mathbf{U}$, and the set of n scalar eigenvalues λ_i forming the diagonal matrix $\mathbf{\Lambda}$. These are found as the solution of the equation(s):

$$\mathbf{A} \cdot \mathbf{U} = \mathbf{U} \cdot \mathbf{\Lambda} \qquad (1)$$

Note that adjacency matrices of the available benchmark graphs are not symmetric, *i.e.* graphs are directed. Thus, $\mathbf{A}$'s eigenvalues and eigenvectors are complex-valued, and only *right* eigenvectors are considered. The set of graph eigenvalues λ_i is of crucial importance to many concepts of system analysis such as stability [8], and -as it will be demonstrated in the remaining of this paper- robustness and fault identification. Fig. 2 shows eigenvalues in the complex plane of the toy circuit. Furthermore, note in the middle and bottom rows of Fig. 2 how an open-circuit and a short-circuit fault can be modelled, *i.e.* how they affect the adjacency

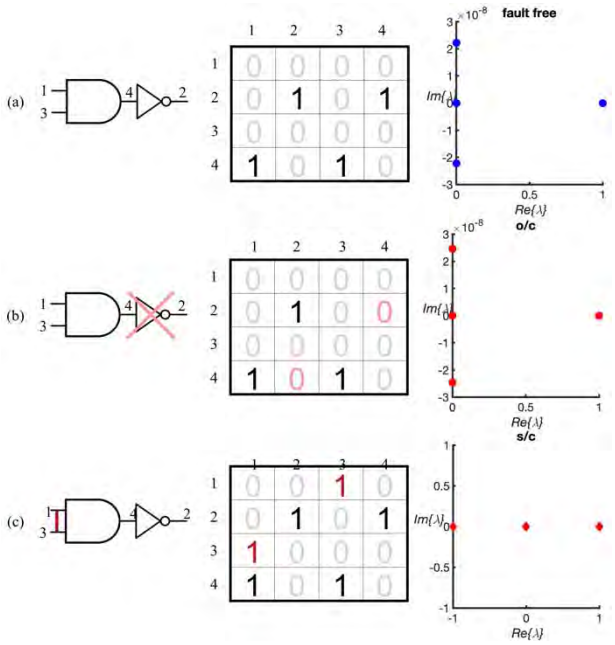

Fig. 2. Schematic of a logic circuit, adjacency matrix of its graph representation, and eigenvalues of the matrix in the case of fault free circuit (a), and in the presence of one open-circuit (b), or short-circuit (c) fault.

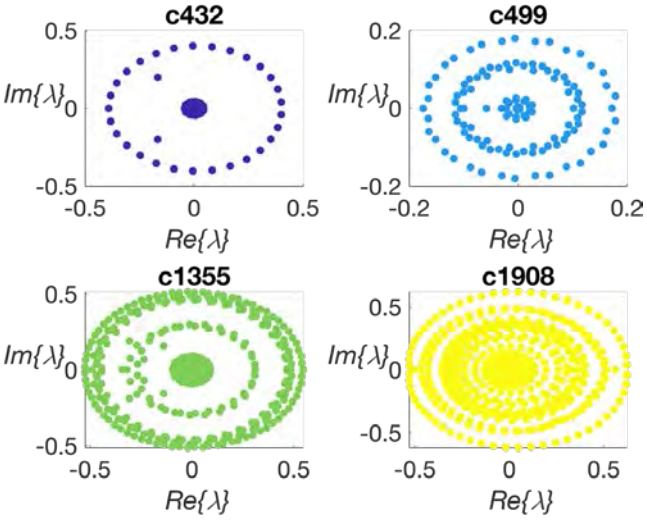

Fig. 3. Eigenvalues of benchmark circuits

matrix and the consequent set of eigenvalues. Both types of faults change the resulting eigenvalue distribution, and in this particular circuit, the effect of short-circuit faults is more prominent.

Moving to the analysis of ISCAS'85 benchmarks, eigenvalue empirical distributions for the fault free, and faulty circuits are reported. Fig. 3 shows the eigenvalues (in the complex plane) of the four used benchmark circuits. The eigenvalues are situated in several concentric circles the number of which, together with the density of λ_i, increases with the graph size n.

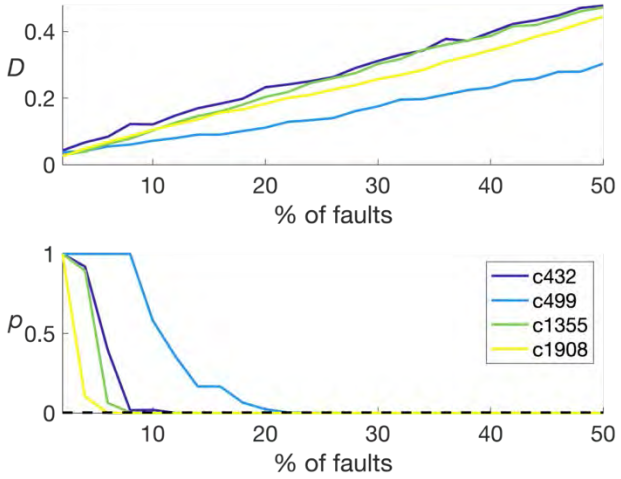

Fig. 4. Kolmogorov-Smirnov statistics (D) and p-values of test on eigenvalue distributions between the original and networks with open-circuit faults.

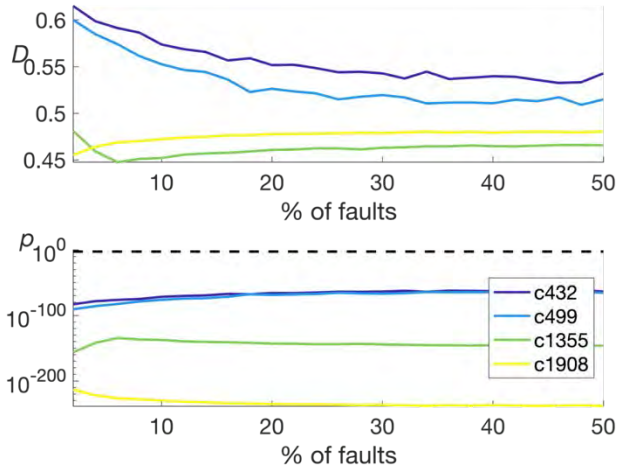

Fig. 5. Kolmogorov-Smirnov statistics (D) and p-values of tests on eigenvalue distributions between the original and networks with short-circuit faults

Two types of faults are considered: short circuit (s/c) and open circuit (o/c). An o/c is "put" in the original circuit by deleting an edge, *i.e.* setting a randomly chosen nonzero entry of $\mathbf{A}$ to 0 (Fig. 2., middle row). Different levels of gravity of the fault are modelled by choosing the number of put open circuits as a percentage of available connections in the network. In a similar fashion, an s/c fault is reflected in adding a certain value on top of an entry of $\mathbf{A}$ regardless of whether there was a nonzero edge or not. In this case, the percentage of faults is calculated *w.r.t.* all possible connections between the network nodes, that is $n(n-1)/2$. The added value is chosen to be equal to 1, so as to model the transfer of one unit of information. Note that in both types of faults, the modification of $\mathbf{A}$ is symmetric since, as opposed to gated connections which are by nature one-directional, o/c and s/c connections are bidirectional.

For each of the values of percentage of faults (from 2 to 50 with step size 2), there were 20 faulty circuits generated. The empirical distribution functions (EDF) of eigenvalues of these circuits are then compared to EDFs of the original circuits in Figs. 4 and 5, and illustrated in Figs. 6 and 7 (up to the fault percentage of 10%). The comparison involved Kolmogorov-Smirnov statistical test designed to determine if there is significant difference between the eigenvalue distributions of the fault free and a faulty circuit. The test rejects the null hypothesis of the same underlying distribution for a high enough value (depending on the chosen significance level α) of the test statistic $D = \sup_t |F_1(t) - F_2(t)|$, where $F_1(t)$ and $F_2(t)$ are empirical cumulative distributions of the given samples. A version of the test extended to 2-dimensional distributions was used here since the eigenvalues are complex in general [9,10]. A high (low) value of Kolmogorov-Smirnov statistic D suggests more (less) distinct probability distributions, further suggesting higher (lower) influence of the faults on the spectral features of the graph.

In the presented analysis, statistical test was performed multiple times, *i.e.* for each of the 4 circuits, each of 25 fault percentages, and for both types of faults, resulting in 200 tests. High number of tests increases the probability of false positive results. Hence, Bonferroni correction was applied before reporting the corresponding p-values. For the desired total significance level of $\alpha = 0.05$, this means that the reference significance level for each test should be $\alpha/200 = 0.0025$. Results of statistical tests are presented in Figs. 4 and 5, including corrected alpha level as dashed black line. For clarity, the p-values in the case of short-circuit faults are given in logarithmic scale (Fig. 5).

Finally, continuing on the observation that a dominant eigenvalue (with much higher magnitude that others) appears in s/c circuits (Fig. 7), the eigendecomposition was performed for single-fault circuits derived from c432 by modifying connections between specific pairs of nodes (red edges in Fig. 1). The magnitudes of eigenvectors corresponding to the emerged dominant eigenvalue are presented in Fig. 8. As it is explained in the following section, these could be exploited for fault identification.

C. Discussion

This subsection discusses how the previously reported results on eigenspectra relate to the concepts of robustness and fault detection in the analysis of electronic circuits. The postulates of linear algebra used as a basis of the following discussion are adapted from [11].

As the circuit flow is modelled with $\boldsymbol{y} = \mathbf{A}\boldsymbol{x}$, the problem of designing a robust circuit, that is, one with robust information flow, relates to the theory of perturbation and matrix sensitivity analysis. If the sensitivity, *i.e.* partial derivative of output signal with respect to circuit topology, is very low, one considers to have a robust circuit – $|\partial \boldsymbol{y}/\partial \boldsymbol{A}| \approx 0$. On the other hand, eigendecomposition of $\mathbf{A}$ provides an alternative model of circuit flow in terms of

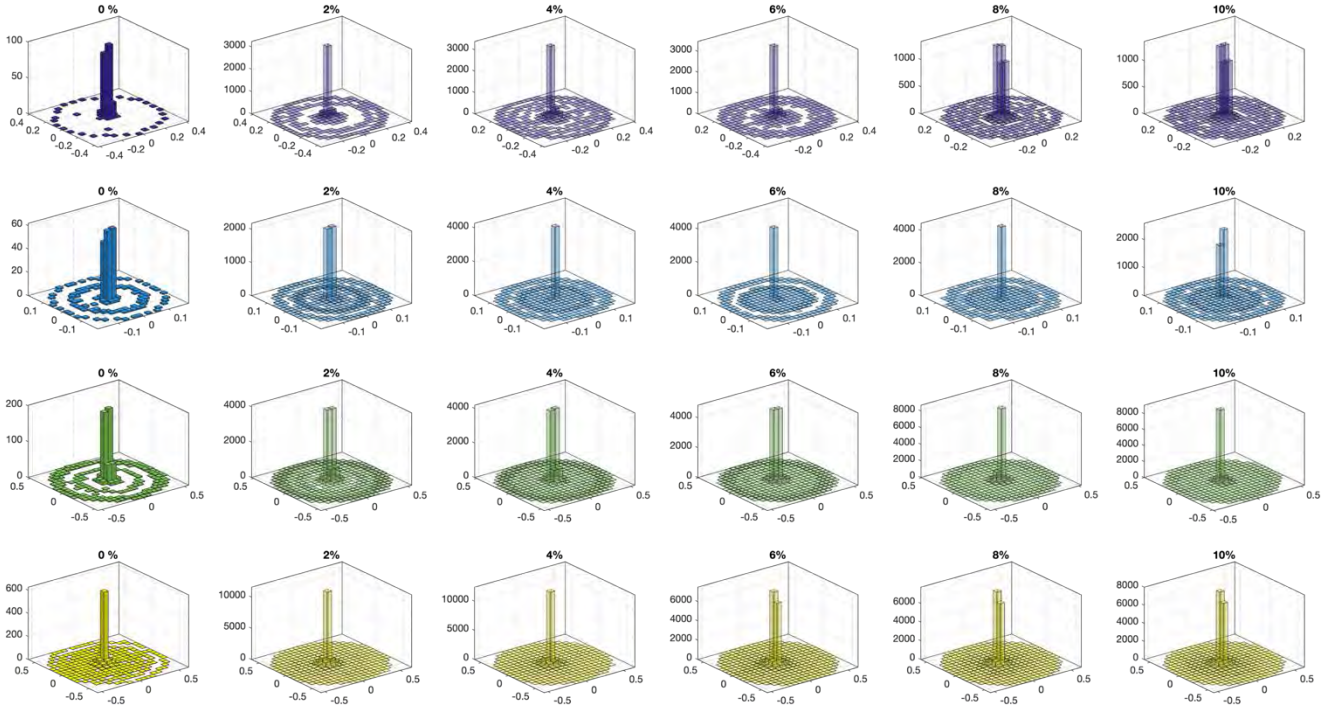

Fig. 6. Histograms of eigenvalues of benchmark circuits (without and with open-circuit faults)

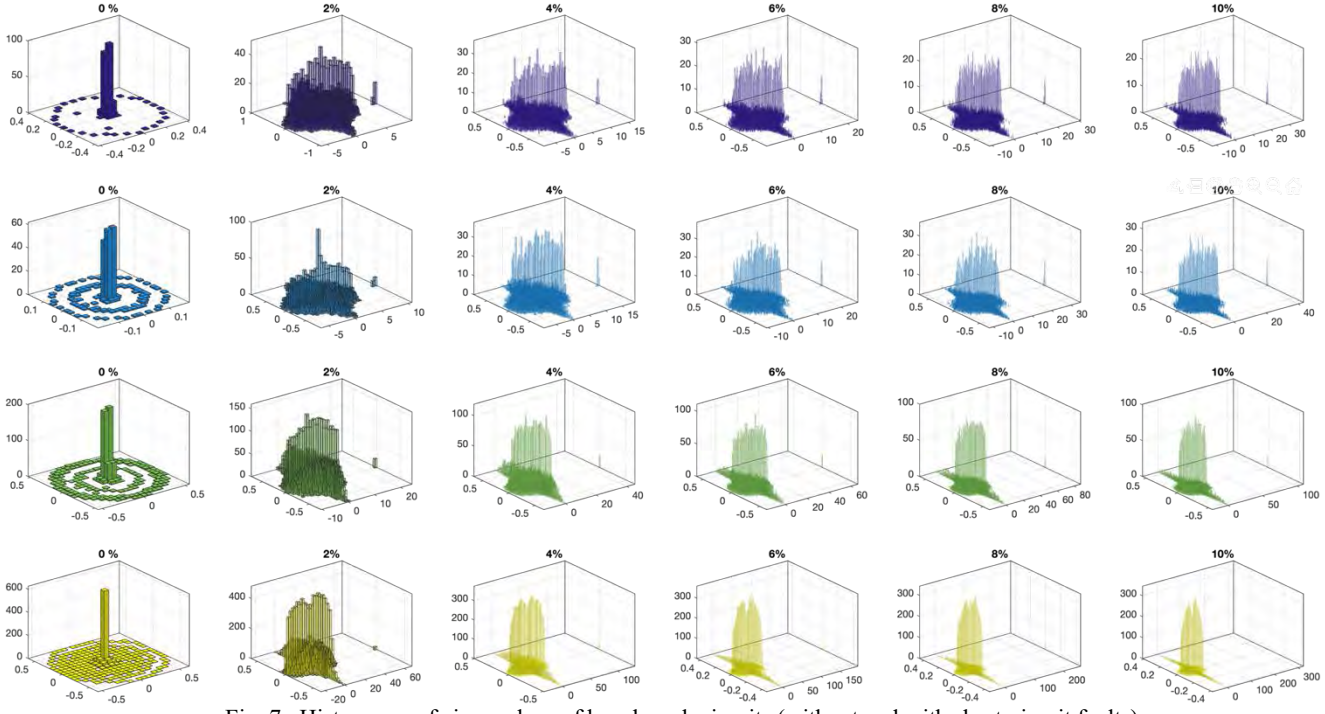

Fig. 7. Histograms of eigenvalues of benchmark circuits (without and with short-circuit faults)

eigenvectors $\boldsymbol{u_i}$ and eigenvalues λ_i as $\boldsymbol{y} = \sum_{i=1}^{n} \lambda_i \boldsymbol{u_i} \boldsymbol{v_i}^T \boldsymbol{x}$, where $\boldsymbol{v_i}$ is a corresponding left eigenvector (for which the matrix form is $\mathbf{V} = \mathbf{U}^{-1}$). Eigenvectors and eigenvalues are in fact functions of each other but for simplicity one can consider the sensitivity of circuit output to be defined by eigenvectors since they can be seen as specific topological principal components of the circuit. Hence, under a small perturbation matrix **E** that models s/c or o/c entries, a robust circuit **A** would be one for which the eigenvectors $\widetilde{\boldsymbol{u}}_i$ of $\boldsymbol{A} + \boldsymbol{E}$ span similar vector subspaces as $\boldsymbol{u_i}$. Of general interest is to find features of circuits **A** which satisfy this property. As seen from the results of statistical testing (Figs. 4 and 5) a significant difference between eigenvalue distributions emerges at the highest percentage of (o/c) faults for c499. In other words, this circuit is the most robust, and its robustness can be related to the initial eigenvalue density. Indeed, from perturbation theory one finds that:

$$\sup\{\mathrm{dist}(\mathrm{span}\{\boldsymbol{u}_i\}, \mathrm{span}\{\widetilde{\boldsymbol{u}}_i\})\} \propto \frac{1}{\min_{j \neq i}\{\lambda_i, \lambda_j\}} \qquad (2)$$

If an eigenvalue is very distant from others, then the upper bound of the distance between the spans of its corresponding eigenvectors of original and perturbed matrices is lower. Hence, for a circuit with highly distinct eigenvalues, the effect faults have on its eigenvectors remain tightly upper-bounded. In other words, the circuit flow is preserved under small changes of its connections. Setting aside the particularly robust c499, a general trend is observed that if the circuit has higher number of nodes it is less robust (the significance is reached for lower percentage of o/c faults – Fig. 4, and *D* has much lower values for low percentages of s/c faults – Fig. 5). This happens since all presented circuits have eigenvalues in more or less similar range and yet higher number of nodes implies higher number of eigenvalues, finally rendering the mutual distances between them lower.

Though actual difference of information flow is reflected in the exact values of eigenvectors and eigenvalues of perturbed matrices, intuitively one can inspect the robustness just by looking at the compact support of the eigenvalue distribution. Hence, it can be observed that the benchmark circuits are much less robust to s/c faults than to o/c faults. Indeed, the support of EDFs with o/c remains circular regardless of the percentage of faults (Fig. 6), whereas the support of EDFs with s/c distorts into a star-shaped or a circular one with prominent tails (Fig. 7).

The high sensitivity to s/c faults (Fig. 5) is partially compensated by the potential ability to detect particular faults, *i.e.* to identify the location (pair of nodes/vertices) where the fault originates. Indeed, Fig. 7 shows that in presence of s/c faults the circuits exhibit a dominant eigenvalue with magnitude much higher than all others. Even though the output $\boldsymbol{y}$ is often completely destroyed with just a single-connection fault, the particular distribution of eigenvalues provides a way to (partially) identify the fault. This can be explained by the power iteration, a method for

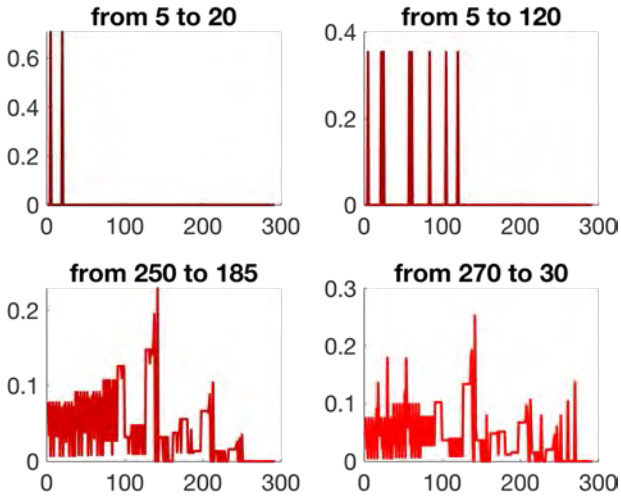

Fig. 8. Magnitude of dominant eigenvectors in cases of single short-circuit faults (red edges in Fig. 1)

calculating the eigenvector corresponding to the dominant eigenvalue (assuming $|\lambda_1| > |\lambda_2| \geq \ldots \geq |\lambda_n|$). With k iterations, the vector $\boldsymbol{x}^{(k)} = \mathbf{A}^k \boldsymbol{x}$ converges to the eigenvector $\boldsymbol{u_1}$ regardless of the input $\boldsymbol{x}$. There is a condition to be satisfied that $\boldsymbol{x}$ should contain a component in the direction of the dominant eigenvector ($\boldsymbol{x}$ not orthogonal to $\boldsymbol{u_1}$), but this condition is almost surely satisfied in practice. It is known that the distance between spans of the eigenvector $\boldsymbol{u_1}$ and its k-iterated approximation $\widehat{\boldsymbol{u}}_1^{(k)}$ is of order of magnitude that depends on the ratio between the two highest-magnitude eigenvalues:

$$\mathrm{dist}\left\{\mathrm{span}\{\boldsymbol{u_1}\}, \mathrm{span}\left\{\widehat{\boldsymbol{u}}_1^{(k)}\right\}\right\} = O\left(\left|\frac{\lambda_2}{\lambda_1}\right|^k\right) \qquad (3)$$

Indeed, if the dominant eigenvalue λ_1 has significantly higher magnitude than its successor λ_2 , the algorithm can reach convergence in just one iteration, implying that

$$\boldsymbol{y} = \mathbf{A}\boldsymbol{x} \approx \boldsymbol{u_1} \neq f(\boldsymbol{x}) \qquad (4)$$

This stable circuit output (at all considered nodes), that does not depend on the input vector $\boldsymbol{x}$, can be seen as a particular distribution of information driven by an internal connection fault (obstructed flow in case of o/c, enhanced flow in case of s/c). However, since a different location of an s/c fault may induce a different output in Eq. (4), one can identify the fault's location by recognizing the signature of the particular output, previously simulated as the dominant eigenvector. These eigenvectors are plotted in Fig. 8 for particular locations of faults (Fig. 1) in c432. As the eigenspectra are complex-valued in general, only the magnitudes are plotted here as an approximation of the real-world output that would be generated as a consequence of the fault. For shown faults, dominant eigenvectors can clearly be distinguished, allowing for the fault identification. However, in general, the dominant eigenvector as simulated

here may be quite similar for two or more different single s/c faults. Still, this simulation provides at least a way to reduce the number of possible locations of a fault.

Since the considered eigenvectors are of the same nature as the graph model, *i.e.* the information flow, and not circuit function, a question is raised on how to measure them in practice during a physical test. In order to have physical measurements of the information flow in the circuit, one needs to simulate the propagation of a signal throughout the circuit unconstrained by the particular gates. Conceptually, this may be accomplished by exploiting the RF (radio-frequency) features of the circuit. The transistors exhibit parasitic impedances connecting their terminals, meaning that an AC signal of high frequency can be propagated regardless of the DC logic input, as long as the condition for the active operating mode is fulfilled. This may be significantly challenging in an existing circuit, since the AC output at the logic gate may not be the sum of inputs due to different delays imposed by transmission lines and capacitances, and consequently the phase difference. However, the circuit can be originally designed in IC technology in a way that allows the signal of certain frequency to be propagated throughout the circuit. Then, the fault identification would comprise of (a) making a dictionary of faults-to-eigenvectors based on the described methodology, (b), driving the circuit with the AC signal and recording the output (at different probing nodes; not necessarily just at the functional circuit output), and (c) finding the eigenvector closest in form to the recorded signal, ultimately informing about the corresponding fault location from the dictionary. Ideally, the amplitudes of AC signals at probed nodes should reflect the structure of the magnitude of an eigenvector. Analogously, the presence of multiple faults could also be reflected in the (larger) eigenvector dictionary. Implementation of the described fault identification procedure is certainly intricate due to complex behaviour of circuits at high frequencies, and its specific challenges fall beyond the scope of this paper. Nonetheless the method represents a conceptual framework one can explore further for practical use in testing and design for testability.

III. Conclusion

This paper provided insight into parallels between matrix algebra on graphs and logic circuits' (represented by graphs) robustness and capability of fault identification. Main advantages of the described simulation approaches are (a) availability of a general measure of robustness (percentage of faults at which divergence between eigenvalue distributions gets statistically significant) appropriate for comparing electrical networks of different size and function, and (b) possibility to -through a look-up table (fault location → dominant eigenvector)- ease the fault diagnostics (detection and identification).

On the other hand, certain limitations exist that need to be addressed before further extensions of the described approach: (a) computation of eigendecomposition of very sparse graphs (number of edges few orders of magnitudes lower than number of vertices) may be numerically unstable; (b) in the current form, the graphs are described with binary adjacency matrices thus hindering the possible modelling of partially obstructed flow (degrading/aging components); (c) the RF approach to fault identification needs to be extended from the conceptual to practical framework. Hopefully, work in this area will provide a fully functional framework for exploration of logic circuits' robustness, reliability, and similar concepts.

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