OTA-C Filter Synthesis Based on Existing LC Solutions

Vančo B. Litovski, Jelena Milojković, and Miljana Milić

Abstract: The problem of synthesis of high frequency analog integrated CMOS circuits is visited. Theory is developed and implementation demonstrated for synthesis of analog OTA-C (or GM-C) filters based on existing low-pass LC solutions. Instructive example is given produced by the *RM* software for filter design. This report may be considered as a case study supported by a rather complex design example.

Keywords – Filter design, OTA-C filters, Gm-C filters, CMOS integrated filters, High frequency filters, Cascade circuit synthesis.

I. Introduction

One of the problems encountered in high frequency analog integrated filter production is the area needed to produce an inductor. It is realized in a form of a flat spiral line the inductance of which is limited not only by the area but by its huge parasitic capacitance. One such inductor realized in CMOS was reported in [1].

The most important electrical parameters of an integrated inductor are the inductance (L), its resistance (R), its parasitic capacitance and its Q-factor (Q) as a secondary parameter. The layout of one inductor of this kind is depicted in Fig. 1a. One may see that the wires are twisted to reduce the parasitic capacitance. This inductor is specific in the sense that it has a tap terminal allowing specific uses. Fig. 1b depicts the dependence of the reactance and the resistance of the integrated inductor on the signal frequency which is an additional problem when designing filters with this kind of components. The numerical values of the equivalent circuit depicted in Fig. 1c, at f=2.43 GHz, are i=6 nH, R_S=9.3 Ω, C_S=220 fF and G_S=0.2 mS. The value of the Q-factor is Q=8.33.

To avoid such a component, attempts were made to find an active circuit that simulates the inductance good enough to be implemented in high frequency CMOS integrated circuits.

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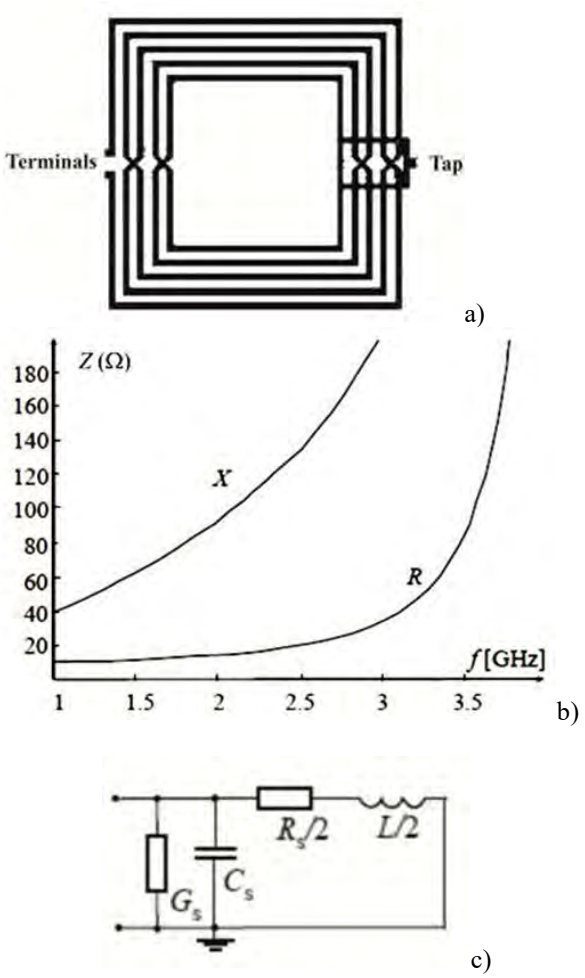

Fig. 1. Planar integrated inductor. a) layout, b) Frequency dependence of the impedance, and c) Equivalent circuit of the half of the inductor

There are many solutions offering a simulated inductor using active components and capacitors. These are based on the concept of NIC (negative impedance converter) which will be not elaborated further here as a general circuit theoretical issue. The main difference in all such circuits if high frequencies are planned to be used is related to the active component. Namely, the CMOS operational amplifier (OA) performance is not good enough for these purposes so that the OTA (operational transconductance amplifier) took over. Based on that solutions were found for the simulated inductances [2][3] of which we will later on elaborate the one based on gyrators [4] and described in [5].

The OTA itself is not perfect, too. Its main characteristics are the frequency dependence of its transconductance and

output capacitance. Ideally, one would like to have a perfect OTA which means a component with zero valued output capacitance and frequency independent controllable transconductance. There is no such perfect component, however, despite the fact that improvements are reported almost on daily basis [6]. As an example Fig. 2 depicts the frequency dependence of the transconductance of an OTA [7] obtained by simulation while Fig. 3 depicts the corresponding output impedance. As can be seen high frequencies are reached (cut-off frequency is claimed to be 567 MHz) the transconductance being much more frequency independent than the output impedance. Unfortunately neither the transconductance nor the output impedances is given in absolute values so one is not capable to extract further conclusions.

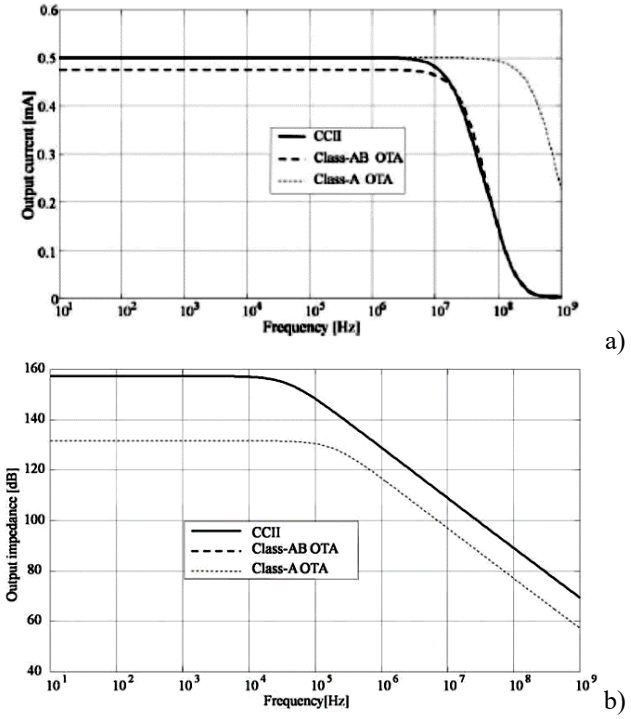

Fig. 2. a) Transconductance and b) Output impedance (modulus) as a function of frequency [7] (Courtesy of the authors)

The fundamental idea of implementation of simulated inductance is based on the availability of LC cascaded circuits which are synthesized by some other filter synthesis software system or even extracted from an existing catalogue such as [8]. In that way the inductors are substituted by an equivalent circuit containing OTAs and a capacitor and the rest of the filter elements (capacitors) remain the same. That, of course, is a very attractive method and even designer with extremely limited knowledge of filter design can produce successful designs.

In this paper we will review very briefly the equivalent circuit to an inductor and demonstrate how the synthesis is functioning. Equivalent circuits to the corresponding LC cells realizing proper transmission zeros will be introduced. The method described here will be tested using ideal OTAs (infinite output impedance) to check for the synthesis process and not for the properties of the practical realization. The example given is rather complicated confirming the effectiveness of the synthesis method. It was produced by the $\mathcal{RM}$ software for filter design [9][10][11].

II. SIMULATING INDUCTORS BY GYRATORS

The fundamental building block which will be used to create the simulated inductor is the gyrator as depicted in Fig. 3.

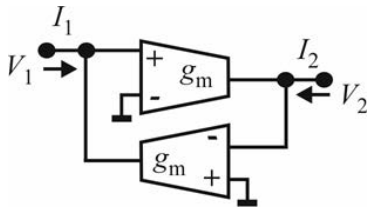

Fig. 3. Gyrator realized by a pair of OTAs

For this circuit the nodal equations are:

$$I_1 = g_m \cdot V_2$$
$$I_2 = -g_m \cdot V_1 \quad (1)$$

When loaded by an impedance Z_L, the output voltage will be:

$$V_2 = -Z_L \cdot I_2 \quad (2)$$

After substitution in (1) one gets

$$I_1 = g_m^2 \cdot Z_L \cdot V_1 \quad (3)$$

For $Z_L = 1/(j\omega C)$, one has

$$I_1 / V_1 = \frac{g_m^2}{j\omega C} = \frac{1}{j\omega L_e} \quad (4)$$

where

$$L_e = C / g_m^2 \quad (5)$$

A gyrator loaded by capacitor will behave as an inductor. Since the capacitor has one terminal grounded the resulting simulated inductor will be grounded, too.

It is up to the designer to decide whether to use a fixed value for the transconductance or for the capacitor in order to create the desired value of the inductance. Namely, the transconductance may be voltage controlled while the voltage digitally created which means that, in general, finer granulation may be achieved. The capacitance is programmed by connecting and disconnecting incremental

capacitances already available on the chip. From the functionality point of view, however, there may be an additional consideration. Namely, one would prefer smaller transconductances since in that case the output impedance is expected to be larger which makes the component nearer to the perfect OTA. If the transconductance is chosen to be variable this opportunity will be not available.

A. Simulating a floating inductor

The schematic depicted in Fig. 4 represents a connection of two gyrators and a capacitor to produce a floating inductor. To show that we will write the nodal equations for the circuit as

$$\begin{aligned} I_1 &= g_m \cdot V_C \\ I_2 &= -g_m \cdot V_C \\ j\omega C \cdot V_C - g_m V_1 + g_m V_2 &= 0 \end{aligned} \tag{6}$$

After eliminating VC from the third equation and having in mind $I_1 = -I_2$, one gets

$$Z_L = \frac{V_1 - V_2}{I_1} = \frac{j\omega C}{g_m^2} \tag{7}$$

This means that the circuit of Fig. 4 behaves as a floating inductor of inductance

$$L_e = C / g_m^2 \tag{8}$$

Note, at ω=0, from (6) one gets $V_1=V_2$ which corresponds to real inductor. The voltage V_C is undefined and so are the currents I_1 and I_2. The last two will be defined by the outer circuit as is the case with the inductor.

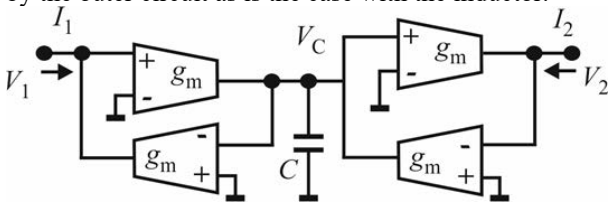

Fig. 4. Floating inductor realized by two gyrators and a capacitor

B. Simulating an ideal transformer

To produce a simulated transformer based on gyrators one may use the circuit of Fig. 5.

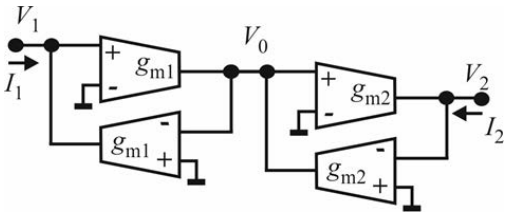

Fig. 5. Transformer simulated by two gyrators

Following are the nodal equations of this circuit

$$\begin{aligned} I_1 &= g_{m1} \cdot V_0 \\ I_2 &= -g_{m2} \cdot V_0 \\ -g_{m1} V_1 + g_{m2} V_2 &= 0 \end{aligned} \tag{9}$$

The transformer's equation is now

$$\frac{V_2}{V_1} = \frac{g_{m1}}{g_{m2}} \tag{10}$$

Note the transformer depicted here has one terminal of both input and output, grounded. That is acceptable for the implementation of the cell realizing complex transmission zero (D-section) depicted in Fig. 14.6b.

Negative "turn-ratio" may be obtained by inverting (interchanging the input terminals of) both transconductance amplifiers in one of the gyrators.

III. GM-C CIRCUIT SYNTHESIS

The circuit synthesis of this kind of filters is straightforward. One is to synthesize first an LC filter using a conventional synthesis procedure using a conventional synthesis program e.g. *cascade_LP* of the *RM* software. Of course, one may use data from catalogues [8] too. The next step is to substitute the inductors and, if necessary, transformers with their models using OTAs. This stem is performed by the *GM_LC* program of the *RM* software. Here we demonstrate the equivalent circuits. A limited set is given to save space. Nevertheless, this set is satisfactory for most physical realizations especially when low-pass circuits are sought.

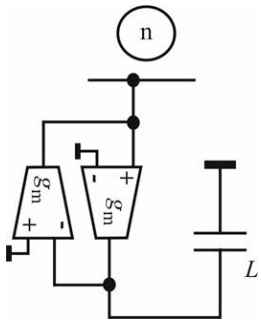

Fig. 6. A grounded simulated inductor

Fig. 6 depicts the equivalent circuit to the grounded inductor. As can be seen from now on the transconductance

is considered a constant while the value of the capacitance is evaluated from (5) to be

$$C = L \cdot g_m^2 \tag{11}$$

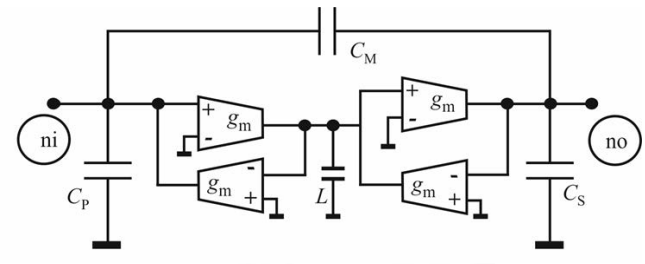

Fig. 7. A cell realizing a transmission zero at the ω-axis

At ω=0 the equivalence is failing since no current flow towards the ground is possible. In the case of synthesis of Gm-C filters based on LC prototypes this problem is usually mitigated by the fact that the inductor is either connected in series with a capacitor or there are two capacitors (to the left and to the right) which disconnect the inductor from DC signals. This will be demonstrated later on by the cell realizing a complex transmission zero without a transformer.

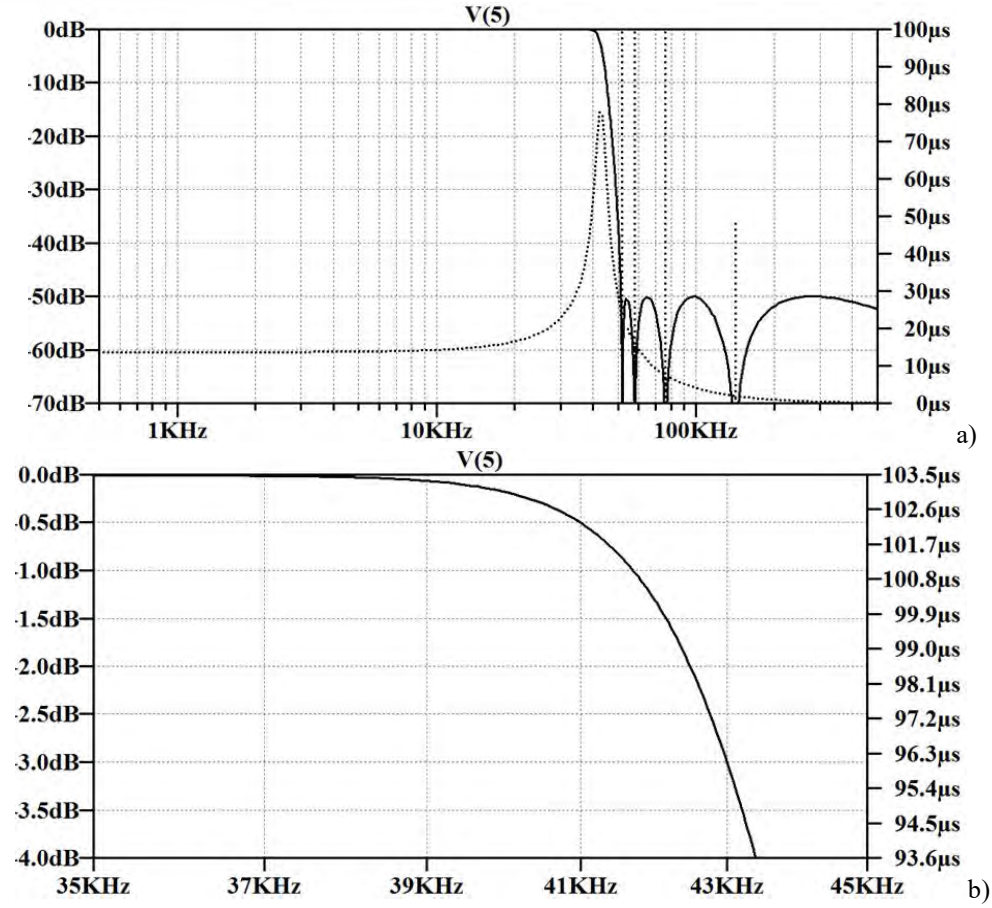

Fig. 8. SPICE simulation results for the example. a) The overall gain and group delay and b) the passband gain at the band edge

This equation may be used as a reference when choosing the value of the transconductance. Namely, a small transconductance e.g. $g_m=10^{-6}$ S, would produce extremely small capacitances. If, for example L=100 µH, one would produce C=0.1 fF which is fairly small value and is in the range of the parasitic capacitances in any CMOS technology. In the opposite case, when large gm is chosen, the resulting capacitance may become very large. For example, if $g_m=10^{-1}$ S, and L=100 µH, one gets C=10 nF. It seems that for this inductance a value of $g_m=10^{-3}$ S, would be preferable. The question is, however, which is the output resistance of such an OTA. If satisfactory, the goal is reached. If not, one must go for a compromise.

Fig. 7 depicts the equivalent circuit to the one realizing a pair of transmission zeros at the ω-axis.

IV. Design Example

As an example a 9th order LSM [9] filter exhibiting a_{max}=3 dB attenuation in the passband will be used. The stopband attenuation was set to a_{min}=50 dB. The cut-off frequency was set to 43 kHz and, as can be seen, g_m= 10^{-6} S was used. The normalized poles an zeros of the transfer function of the LSM filter are given in Table 1. Fig. 8. depicts the SPICE simulation results.

TABLE I. NORMALIZED ZEROS AND POLES OF THE EXAMPLE LSM FILTER

Zeros	
Real part	Imaginary part
0.000000000e+000	±1.207678823e+000
0.000000000e+000	±1.347839032e+000
0.000000000e+000	±1.774177189e+000
0.000000000e+000	±3.290123935e+000

Poles	
Real part	Imaginary part
-7.170315101e-002	±9.991239141e-001
-2.565027588e-001	±9.818358904e-001
-1.451251999e+000	±0.000000000e+000
-5.858625045e-001	±9.061210530e-001
-1.112461676e+000	±6.430061028e-001

To show the schematic of the resulting GM-C filter excepts from the .html report file produced by the GM_LC program are given below.

RM Welcome to The Electronic Filter Design Software

EXTRACTION OF THE CELLS

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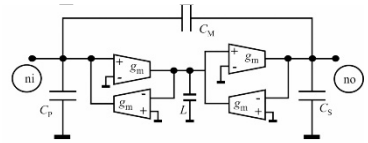
k=1 (th) ZERO AT THE IMAGINARY AXIS=3.2901239e+000

The capacitance (denoted L) within the simulated inductor is L*gm*gm=5.2452831e-013
Cp=2.1382177e-009 Cm=2.4127365e-010 Cs=-2.1680919e-010
Node_i=1 Node_o=2



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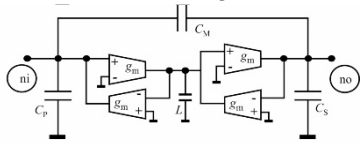
k=2 (th) ZERO AT THE IMAGINARY AXIS=1.7741772e+000

The capacitance (denoted L) within the simulated inductor is L*gm*gm=5.8743338e-013
Cp=6.2896543e-009 Cm=7.4088491e-010 Cs=-6.6280975e-010
Node_i=2 Node_o=3



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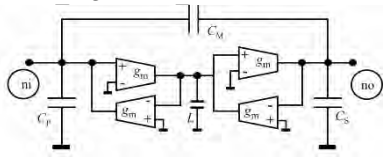
k=3 (th) ZERO AT THE IMAGINARY AXIS=1.3478390e+000

The capacitance (denoted L) within the simulated inductor is L*gm*gm=2.2310528e-013
Cp=6.8013276e-009 Cm=3.3800058e-009 Cs=-2.2579092e-009
Node_i=3 Node_o=4



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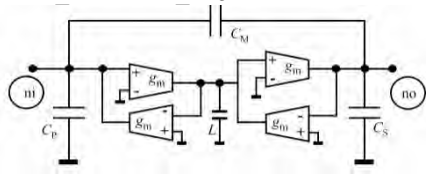
k=4 (th) ZERO AT THE IMAGINARY AXIS=1.2076788e+000

The capacitance (denoted L) within the simulated inductor is L*gm*gm=2.6055821e-014
Cp=-4.4624834e-009 Cm=3.6049205e-008 Cs=5.0929306e-009
Node_i=4 Node_o=5



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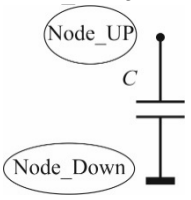
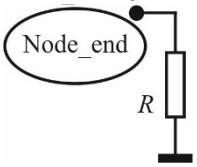
k=5 (th) ZERO AT INFINITY: parallel capacitance C=9.3862427e-010
Node_UP=5 Node_Down=0



----------Residual load impedance----------

Residual is resistor (Implemented in the SPICE description) and R=1.0000000e+003
Node_end=5



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Here ends the synthesis process

V. Conclusion

A case study of synthesis of an low-pass GM-C filter was reported. It was shown that if an LC prototype is available (taken from a catalog e.g. [8] or produced by a dedicated software e.g. [9]) one may easily synthesize a proper GM-C equivalent. The example given here is related to a low-pass filter but, in general, no limitations exist as to where is the location of the passband of the filter. It is our experience [9] that transmission zeros of any kind may be realized by production of GM-C cells equivalent to the ones realized as LCM (M stands for use of transformers). It is our intention to further study the properties of the obtained solution in order to learn on the influence of the imperfections of the OTAs to the properties of the filters.

Acknowledgement

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